WHAT IS CLAIMED IS:

1. An analog to digital converter comprising:

an array of differential input amplifiers, each inputting an input voltage and a corresponding voltage reference, and outputting a differential signal representing a comparison of the input voltage and the corresponding voltage reference;

a plurality of latches storing the differential signal from each of the differential input amplifiers;

a decoder converting the stored differential signals to N-bit digital output;

a first interface amplifier connected to a first edge amplifier of the array through a first cross point; and

a second interface amplifier connected to a second edge amplifier of the array through a second cross point,

wherein the first interface amplifier and the second interface amplifier are connected to each other through a third cross point.

2. The analog to digital converter of claim 1, wherein positive and negative outputs of each differential input amplifier of the array are connected to respective outputs of a neighboring differential input amplifier through corresponding resistors.

3. The analog to digital converter of claim 1, wherein positive and negative outputs of each interface amplifier are connected to respective outputs of the same polarity of a corresponding edge amplifier through corresponding resistors.

4. The analog to digital converter of claim 1, wherein a positive output of the first interface amplifier is connected to a negative output of the second interface amplifier through a first resistor.

5. The analog to digital converter of claim 4, wherein a negative output of the first interface amplifier is connected to a positive output of the second interface amplifier through a second resistor.

6. The analog to digital converter of claim 1, further including a track and hold amplifier inputting a differential input signal and outputting the input voltage to the array, the track and hold amplifier comprising:

a first transistor pair driven by a clk signal at their gates;

a second transistor pair driven by a clkb signal at their gates;

a third transistor pair inputting the differential input signal at their gates through the first and second transistor pair, and having their sources biased by corresponding current sources; and

a replica circuit connected to the gates of the third transistor pair and to substrates of the third transistor pair for biasing wells of the third transistor pair so as to reduce nonlinear well behavior.

7. The analog to digital converter of claim 1, further comprising:

a reference ladder including a plurality of resistors and taps providing the voltage references; and

at least one controllable current source in series with each tap for adjusting the voltage reference of the each tap.

8. An analog to digital converter comprising:

a reference ladder including a plurality of resistors and taps providing voltage references;

at least one controllable current source in series with each tap for adjusting the voltage reference of the each tap;

an array of differential input amplifiers, each inputting an input voltage and a corresponding voltage reference, and outputting a differential signal representing a comparison of the input voltage and the corresponding voltage reference;

a plurality of latches storing the differential signal from each of the differential input amplifiers; and

a decoder converting the stored differential signals to N-bit digital output.

9. The analog to digital converter of claim 8, wherein the analog to digital converter includes a zero crossing generator that inputs the voltage references and outputs them to the array.

10. The analog to digital converter of claim 8, wherein further including a second controllable current source for the each tap, and connected between the tap and a supply rail.

11. A track and hold amplifier inputting a differential input signal and outputting a clocked input signal comprising:

a first transistor pair driven by a clk signal at their gates;

a second transistor pair driven by a clkb signal at their gates;

a third transistor pair inputting the differential input signal at their gates through the first and second transistor pair, and having their sources biased by corresponding current sources; and

a replica circuit connected to the gates of the third transistor pair and to substrates of the third transistor pair for biasing wells of the third transistor pair so as to reduce nonlinear well behavior.

12. The track and hold amplifier of claim 11, wherein the replica circuit includes a fourth pair of transistors whose sources are biased by corresponding replica current sources, and

wherein the sources of the fourth pair of transistors are connected to the corresponding substrates of the third transistor pair and to substrates of their own transistors.